UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,839	03/24/2004	Joseph M. Jeddeloh	33801/US	7961

7590 04/19/2006

Kimton N. Eng, Esq.
DORSEY & WHITNEY LLP
Suite 3400
1420 Fifth Avenue
Seattle, WA 98101

EXAMINER	
FLOURNOY, HORACE L	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/809,839	JEDDELOH ET AL.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/24/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,7-10,12-14,17-19 and 22-36* is/are rejected.

7)☒ Claim(s) *3,5,6,11,15,16,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/21/2006, 8/23/2005, 7/25/2005, 6/24/2005, 4/25, 2005, 2/22/2005 5/20/2004, 6/01/2004, 3/24/2004*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. **10/809,839** has a total of *36* claims pending in the application; there are *10* independent claims and *26* dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

As required by **M.P.E.P.** 609(c), the applicant's submission of the Information Disclosure Statements dated **3/21/2006, 8/23/2005, 7/25/2005, 6/24/2005, 4/25/2005, 2/22/2005, 8/20/2004, 6/01/2004, and 3/24/2004** are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P.** 609(c), a copy each PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 4, 7-10, 12-14,17-19, 22-36 are rejected under 35 U.S.C. 102(e) as being anticipated by **Meyer et al. (U.S PG Publication No. 2005/0086441 hereafter referred to as Meyer)**.

With respect to **independent claims 1, 8, 12,**

> *"A method of responding to a read request in a system memory having a responding memory hub* **[Meyer discloses this limitation in FIG. 1, element 140 (see all associated text for element 140 of FIG.1)]** *and at least one interposing memory hub through which a read response is transmitted on a data path* **[disclosed, e.g. in FIG. 1, element 134]** *of the interposing memory hub,* **[Meyer discloses this limitation in FIG. 1, element 132 (see all associated text for element 132 of FIG.1)]** *the method comprising: retrieving read data from a memory device coupled to the responding memory hub and preparing a read response including the read data;* **[Meyer discloses in paragraph [0006], "A**

memory response is typically provided only for a read memory request, and typically includes read data as well as an identifying header that allows the memory hub controller to identify the memory request corresponding to the memory response."] *generating an arbitration packet including data indicative of a data path configuration for the read response; providing the arbitration packet and the read response to the interposing memory hub,* **[Meyer discloses these limitations, e.g. in paragraph [0019], "In operation, each memory hub 140 executes a desired arbitration process to control the way in which local and downstream responses are returned to the memory hub controller 132."]** *the arbitration packet provided prior to the read response; and receiving the arbitration packet at the interposing memory hub,* **[this limitation is disclosed, e.g. in paragraph [0024]]** *decoding the data of the arbitration packet* **[Meyer discloses in paragraph [0022], "The specific operation of the arbitration control logic 210 in controlling the multiplexer 208 to provide responses from one of the queues 202, 206..."** *and enabling a data path for the read response in the interposing memory hub in accordance with the data of the arbitration packet."* **["...or the bypass path 204 depends on the particular arbitration process being executed by the control logic."]**

With respect to **independent claim 18**,

"A method of communicating between a first and second memory hub for configuring a data path in the second memory hub, the method comprising: generating an arbitration packet for an associated read response to be coupled through the second memory hub, **[Meyer discloses these limitations, e.g. in**

paragraph [0019], **"In operation, each memory hub 140 executes a desired arbitration process to control the way in which local and downstream responses are returned to the memory hub controller 132."]** *the arbitration packet having a command code field including data identifying that it is an arbitration packet and further having a data path field including data indicative of a data path configuration in the second memory hub;* **[Meyer discloses in paragraph [0006], "A memory response is typically provided only for a read memory request, and typically includes read data as well as an identifying header that allows the memory hub controller to identify the memory request corresponding to the memory response."]** *transmitting the arbitration packet prior to transmitting the associated read response to the second memory hub;* **[Meyer teaches in paragraph [0022], "The arbitration control logic 210 gives priority to downstream responses, and as a result the hub 140 in module 130b forwards upstream the downstream responses C1 first and thereafter forwards upstream the local response B1 as shown in FIG. 3." As stated supra, the examiner interprets *arbitration packet* sited by the applicant is analogous to certain types of responses and where they are directed as taught by Meyer. Meyer teaches that a memory hub can receive an arbitration packet prior to sending an associated read response.]** *and configuring the data path in the second memory hub in accordance with the data included in the data path field."* **[disclosed, e.g. in paragraphs [0021] and [0022].]**

With respect to **independent claim 22**,

"A memory hub coupled to at least one memory device, **[See Meyer FIG.1]** *the memory hub comprising: remote and local input nodes; an output node; a configurable data path coupled to the remote and local input nodes and further coupled to the output node,* **[See Meyer FIGs. 1 and 2 and all associated text from the specification]** *the configurable data path operable to couple at least one of a read response coupled through the remote and local input nodes to the output node;* **[See Meyer FIGs. 1 and 2 and all associated text from the specification]** *and an arbitration control circuit coupled to the configurable data path, the output node, and the remote input node, the arbitration control circuit operable to generate an arbitration packet for an associated read response coupled through the local input node,* **[See Meyer FIGs. 1 and 2 and all associated text from the specification. Note FIG.2, element 210 and associated text]** *the arbitration packet including data indicative of a data path configuration for the associated read response, the arbitration control circuit further operable to configure the configurable data path in accordance with the data included with an arbitration packet coupled thorough the remote input node in preparation of coupling an associated read response coupled through the remote input node to the output node."* **[Meyer discloses this limitation e.g. in paragraphs [0022] and [0023].]**

With respect to **independent claim 25**,

"A memory hub, comprising: a bypass data path coupled between an input node and an output node on which read responses are coupled there between in

response to being enabled; **[See Meyer FIGs. 1 and 2 and all associated text from the specification]** *and an arbitration control circuit coupled to the bypass data path operable to generate an arbitration packet in response to retrieving read data from a memory device coupled to the memory hub,* **[See Meyer FIGs. 1 and 2 and all associated text from the specification. Note FIG.2, element 210 and associated text]** *the arbitration packet having a data path field including activation data to enable a bypass data path of an upstream memory hub, the arbitration control circuit further operable to receive an arbitration packet from a downstream memory hub and enable the bypass data path to couple a read response received therefrom from the input node to the output node."* **[Meyer discloses this limitation e.g. in paragraphs [0022] and [0023].]**

With respect to **independent claim 27**,

"A memory module, comprising: a plurality of memory devices; **[See Meyer FIG.1, elements 130 a, b, n]** *and a memory hub* **[See Meyer FIG.1, element 140]** *the coupled to the memory devices through a memory device bus to access the memory devices,* **[See Meyer FIG.1, element 150]** *the memory hub comprising: remote and local input nodes, the local input node coupled to the memory device bus; an output node;* **[See Meyer FIGs. 1 and 2 and all associated text from the specification. Note FIG.2, element 210 and associated text]** *a configurable data path coupled to the remote and local input nodes and further coupled to the output node,* **[See Meyer FIGs. 1 and 2 and all associated text from the specification]** *the configurable data path operable to couple at least one of a read response coupled through the remote and local*

input nodes to the output node; **[Meyer discloses in paragraph [0022], "The specific operation of the arbitration control logic 210 in controlling the multiplexer 208 to provide responses from one of the queues 202, 206 or the bypass path 204 depends on the particular arbitration process being executed by the control logic."]** *and an arbitration control circuit coupled to the configurable data path, the output node, and the remote input node, the arbitration control circuit operable to generate an arbitration packet for an associated read response coupled through the local input node,* **[See Meyer FIG. 2, element 210]** *the arbitration packet including data indicative of a data path configuration for the associated read response, the arbitration control circuit further operable to configure the configurable data path in accordance with the data included with an arbitration packet coupled thorough the remote input node in preparation of coupling an associated read response coupled through the remote input node to the output node."* **[Meyer discloses this limitation e.g. in paragraphs [0022] and [0023].]**

With respect to **independent claim 30**,

"A memory module, comprising: a plurality of memory devices; **[See Meyer FIG.1, elements 130 a, b, n]** *and a memory hub coupled to the memory devices through a memory device bus to access the memory devices,* **[See Meyer FIG.1, elements 140]** *the memory hub comprising: a bypass data path coupled between an input node and an output node on which read responses are coupled there between in response to being enabled;* **[disclosed in paragraph[[0023], "...the bypass path 204 in the hub 140..." See FIG.2, element 204]** *and an*

arbitration control circuit coupled to the bypass data path operable to generate an arbitration packet in response to retrieving read data from a memory device coupled to the memory hub, **[See FIG.2, element 210]** *the arbitration packet having a data path field including activation data to enable a bypass data path of an upstream memory hub, the arbitration control circuit further operable to receive an arbitration packet from a downstream memory hub and enable the bypass data path to couple a read response received therefrom from the input node to the output node.* **[Meyer discloses this limitation e.g. in paragraphs [0022] and [0023].]**

With respect to **independent claims 35 and 32**,

"A processor-based system, comprising: a processor having a processor bus; **[FIG. 1, elements 104 and 106]** *a system controller coupled to the processor bus,* **[FIG. 1, element 110]** *the system controller having a peripheral device port,* **[FIG. 1, elements 110, 118, 112]** *the system controller further comprising a controller coupled to a system memory port;* **[FIG. 1, element 132]** *at least one input device coupled to the peripheral device port of the system controller;* **[FIG. 1, element 118]** *at least one output device coupled to the peripheral device port of the system controller;* **[FIG. 1, element 120]** *at least one data storage device coupled to the peripheral device port of the system controller;* **[FIG. 1, element 124]** *a memory bus coupled to the system controller for transmitting memory requests and responses thereon;* **[FIG. 1, element 134]** *and a plurality of memory modules coupled to the memory bus,* **[FIG. 1, element 130]** *each of the modules having: a plurality of memory devices;* **[FIG. 1, element 148]** *and a*

memory hub coupled to the memory devices through a memory device bus to access the memory devices, **[FIG. 1, element 140]** *the memory hub comprising: a bypass data path coupled between an input node and an output node on which read responses are coupled there between in response to being enabled;* **[Meyer discloses in paragraph [0021] a "bypass data path". See FIG. 2, element 204.]** *and an arbitration control circuit coupled to the bypass data path operable to generate an arbitration packet in response to retrieving read data from a memory device coupled to the memory hub,* **[FIG. 2, element 210, "Arbitration Control Logic"]** *the arbitration packet having a data path field including activation data to enable a bypass data path of an upstream memory hub, the arbitration control circuit further operable to receive an arbitration packet from a downstream memory hub and enable the bypass data path to couple a read response received therefrom from the input node to the output node."* **[Meyer discloses this limitation e.g. in paragraphs [0022] and [0023].]**

With respect to **claims 2, 13, 24, 29, 34,**

"The method of claim 1 wherein generating an arbitration packet comprises generating data for the arbitration packet that is used to distinguish the arbitration packet from a read response." **[Meyer discloses in paragraph [0006],"A memory response is typically provided only for a read memory request, and typically includes read data as well as an identifying header that allows the memory hub controller to identify the memory request corresponding to the memory response." Furthermore, Meyers discloses in paragraph [0008], "Each hub must determine whether to send local responses first or**

to forward responses from downstream memory hubs first, and the way in which this is done affects the actual latency of a specific response, and more so, the overall latency of the system memory. This determination may be referred to as arbitration, with each hub arbitrating between local requests and upstream data transfers." As interpreted by the examiner, *arbitration packet* sited by the applicant is analogous to certain types of responses and where they are directed as taught by Meyer.]

With respect to **claims 4, 7, 9, 14, 17, and 19,**

"The method of claim 1 wherein enabling the data path for the read response comprises enabling a bypass data path in the interposing memory hub **[disclosed in paragraph[[0023], "...the bypass path 204 in the hub 140..."]** *to couple the arbitration packet and read response through the interposing memory hub."* **[Meyer teaches this limitation in paragraph [0023]]**

With respect to **claim 10**,

"The method of claim 8, further comprising coupling the arbitration packet to the configured data path for transmitting the same to the receiving memory hub prior to transmitting the associated read response." **[Meyer teaches in paragraph [0022], "The arbitration control logic 210 gives priority to downstream responses, and as a result the hub 140 in module 130b forwards upstream the downstream responses C1 first and thereafter forwards upstream the local response B1 as shown in FIG. 3." As stated supra, the examiner interprets *arbitration packet* sited by the applicant is analogous to certain**

types of responses and where they are directed as taught by Meyer. Meyer teaches that a memory hub can receive an arbitration packet prior to sending an associated read response.]

With respect to **claims 23, 26, 28, 31, 33, and 36,**

"The memory hub of claim 22 wherein the configurable data path comprises: a multiplexer having an output coupled to the output node and a control node coupled to the arbitration control circuit; **[FIG. 2, elements 134, 208, 210, and all associated text within the specification]** *a bypass data path coupled to the remote input node and a first input of the multiplexer;* **[Meyer discloses in paragraph [0021] a "bypass data path". See FIG. 2, element 204.]** *a local queue having an input coupled to the local input node and further having an output coupled to a second input of the multiplexer;* **[Meyer discloses in FIG. 2, element 202: "Local Queue". See all associated text.]** *and a remote queue having an input coupled to the remote input node and further having an output coupled to a third input of the multiplexer,* **[Meyer discloses in FIG. 2, element 206: "Buffered Queue". See all associated text. According to the applicant's specification in paragraph [0019], this remote queue identical to element 206 in FIG. 2 of Meyer.]** *the arbitration control circuit* **[FIG. 2, element 210, "Arbitration Control Logic"]** *operable to generate a control signal for the multiplexer to selectively couple the bypass data path, local queue, or remote queue to the output node."* **[Meyer discloses in the abstract, "A multiplexer is coupled to the local queue, buffered queue, and the bypass path and outputs responses from a selected one of the queues or the bypass path**

responsive to a control signal. Arbitration control logic is coupled to the multiplexer and the queues and develops the control signal to control the response output by the multiplexer."]

Allowable Subject Matter

Claims 3, 5-6, 11, 15-16, 20-21, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

CONCLUSION

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Reginald D. Bragdon

REGINALD G. BRAGDON
PRIMARY EXAMINER

Horace L. Flournoy

Patent Examiner

Art unit: 2189

Supervisory Patent Examiner

Technology Center 2100